

IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Claim 1 (Currently Amended) A queue control device comprising:

a first storage area configured to store a first and a second queue, said first queue including first elements, each of said first elements having an address specifying a next element of the first elements, and said second queue including second elements, each of said second elements having an address specifying a next element of the second elements, wherein a head address of the second queue is stored in a tail element of the first elements, and a tail address of the first queue is stored in a tail element of the second elements;

a second storage area configured to store first pointer information and second pointer information, said first pointer information being a head address specifying a head element of the first elements included in said first queue, and said second pointer information being a tail address specifying a tail element of the second elements included in said second queue; and

a controller which is operatively connected to the first and second storage areas, controller sets ~~an address~~ a head address specifying a head element of the second elements included in said second queue in the tail element of the first elements included in said first queue stored in said first storage area and sets ~~an address~~ a tail address specifying a tail element of the first elements included in said first queue in a tail element of the second elements included in said second queue when the second queue connects to the first queue, wherein the controller controls said first and second queues according to said first pointer information and second pointer information stored in said second storage area.

**Claim 2 (Original)** The queue control device according to claim 1, wherein said controller, when said first queue is absent, sets not only an address specifying the head element in said second queue as said first pointer information in said second storage area but also first information indicating that said first queue is absent in the tail element in said second queue in said first storage area.

**Claim 3 (Original)** The queue control device according to claim 1, wherein said controller, when said second queue is absent, sets not only an address specifying the tail element in said first queue as said second pointer information in said second storage area but also second information indicating that said second queue is absent in the tail element in said first queue in said first storage area.

**Claim 4 (Original)** The queue control device according to claim 1, wherein said second storage area stores a plurality of pieces of said first pointer information and a plurality of pieces of said second pointer information.

**Claim 5 (Original)** The queue control device according to claim 1, wherein said first queue is given higher priority than said second queue.

**Claim 6 (Original)** The queue control device according to claim 1, wherein said first storage area stores the number of a virtual channel according to each of said elements.

**Claim 7 (Previously Presented)** The queue control device according to claim 6, wherein said controller is connected to a transmission control circuit, said transmission

control circuit outputting a virtual channel according to a number of a virtual channel supplied from said controller.

8. (Currently Amended) A queue control device comprising:

a first storage area configured to store a plurality of queue groups, each of said queue groups including a first and a second queue, said first queue including first elements, each of said first elements having an address specifying a next element of the first elements, and said second queue including second elements, each of said second elements having an address specifying a next element of the second elements, wherein a head address of the second queue is stored in a tail element of the first elements, and a tail address of the first queue is stored in a tail element of the second elements;

a second storage area configured to store a time table, said time table including a plurality of time entries, each of said time entries having first pointer information and second pointer information, said first pointer information being a head address specifying the head element in said first queue in each of said queue groups and said second pointer information being a tail address specifying the tail element in said second queue in each of said queue groups; and

a controller which is operatively connected to the first and second storage areas, controls said first and second storage areas and which sets not only an address a head address specifying the head element of the second elements included in said second queue in the tail element of the first elements included in said first queue in each of said queue groups stored in said first storage area but also an address a tail address specifying the tail element of the first elements included in said first queue in the tail element of the second elements in said second queue and controls each of said first and second queues according to said first pointer

information and second pointer information when the second queue connects to the first queue.

**Claim 9 (Original)** The queue control device according to claim 8, wherein said controller, when said first queue is absent in each of said queue groups, sets not only an address specifying the head element in said second queue as said first pointer information in said second storage area but also first information indicating that said first queue is absent in the tail element in said second queue in said first storage area.

**Claim 10 (Original)** The queue control device according to claim 8, wherein said controller, when said second queue is absent in each of said queue groups, sets not only an address specifying the tail element in said first queue as said second pointer information in said second storage area but also second information indicating that said second queue is absent in the tail element in said first queue in said first storage area.

**Claim 11 (Original)** The queue control device according to claim 8, wherein said first queue is given higher priority than said second queue in each of said queue groups.

**Claim 12 (Original)** The queue control device according to claim 8, wherein said first storage area stores the number of a virtual channel according to each of said elements in each of said queue groups.

**Claim 13 (Previously Presented)** The queue control device according to claim 12, wherein said controller is connected to a transmission controller, said transmission controller

outputting a virtual channel according to said number of a virtual channel supplied from said controller.

Claim 14 (Currently Amended) A queue control method including a first queue composed of a first elements, each of said first elements having an address specifying the next element of the first elements, and a second queue composed of a second elements, each of said second elements having an address specifying the next element of the second elements, the queue control method for connecting the first queue and the second queue comprising:

setting a head address specifying the head element of the second elements included in said second queue in the tail element of the first elements included in said first queue;

setting a tail address specifying the tail element of the first elements included in said first queue in the tail element of the second elements included in said second queue;

storing first pointer information specifying the head address in said first queue in a storage area[, ,]; and

storing second pointer information specifying the tail address of said second queue in the storage area.

Claim 15 (Original) The queue control method according to claim 14, further comprising the step of, when said first queue is absent, setting not only an address specifying the head address in said second queue as said first pointer information but also first information indicating that said first queue is absent in the tail element in said second queue.

Claim 16 (Original) The queue control method according to claim 14, further comprising the step of, when said second queue is absent, setting not only an address specifying the tail address in said first queue as said second pointer information but also second information indicating that said second queue is absent in the tail element in said first queue.

Claim 17 (Original) The queue control method according to claim 14, wherein the priority of said first queue is set higher than that of said second queue.

Claim 18 (Original) The queue control method according to claim 14, wherein said elements in said first and second queues are allocated the numbers of virtual channels in a one-to-one correspondence.

Claim 19 (Previously Presented) The queue control device according to claim 1, wherein when separating the first queue and second queue, the controller reads the tail address of the first queue stored in the tail element of the second queue by the second pointer information of the second storage area, and reads the head address of the second queue specified by the tail address read from the tail element of the second queue.

Claim 20 (Previously Presented) The queue control device according to claim 8, wherein when separating the first queue and second queue, the controller reads the tail address of the first queue stored in the tail element of the second queue by the second pointer information of the second storage area, and reads the head address of the second queue specified by the tail address read from the tail element of the second queue.

Claim 21 (Previously Presented) The queue control method according to claim 14, further comprising when separating the first queue and second queue, reading the tail address of the first queue stored in the tail element of the second queue by the second pointer information of the storage area, and reading the head address of the second queue specified by the tail address read from the tail element of the second queue.

22. (New) The queue control device according to claim 1, wherein the second storage area has no tail address specifying the tail element of the first queue and no head address specifying the head element of the second queue.

23. (New) The queue control device according to claim 8, wherein the second storage area has no tail address specifying the tail element of the first queue and no head address specifying the head element of the second queue.

24. (New) The queue control method according to claim 14, wherein in the storing steps, no tail address in the first queue is stored in the storage area no head address in the second queue is stored in the storage area.